CLAIMS:

1. A semiconductor wafer (1) having a multitude of chips (5), of which chips (5) each one of a given number of chips (5) is situated in one of a multitude of adjacent exposure fields (2), and having process control modules (4) which are each arranged in a given area on the semiconductor wafer (1), in which the given areas are formed by the exposure fields (2), and in which each process control module (4) takes the place of at least one chip (5).

2. A semiconductor wafer (1) as claimed in claim 1, in which a process control module (4) is present in each one of at least 25 % of all the exposure fields (2), and in which the process control modules (4) are situated at equal distances from each other with respect to two mutually perpendicular coordinate directions (7, 8).

3. A semiconductor wafer (1) as claimed in claim 2, in which a process control module (4) is present in each exposure field (2).

4. A semiconductor wafer (1) as claimed in claim 1, in which all the process control modules (4) are each situated at the same location (6) in the respective exposure fields (2).